Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims in the application.

Listing of Claims

1. (canceled)

2. (currently amended) An apparatus for processing N number of input signals having a common frequency and chip rate, said apparatus comprising:

at least N number of modulators for modulating N of said N number of input signals into N number of modulated signals;

a combiner for combining said modulated signals into an aggregate signal;

a demux element for decombining said aggregate signal into N number of constituent modulated signals; and

at least N number of demodulators for demodulating each of said N number of constituent modulated signals into N number of recovered signals each corresponding substantially identically to one of said N number of input signals;

wherein said demux element includes ~~a~~ N-1 splitters, a delay element associated with each splitter, ~~line~~ each delay element having one or more switches for switching in a delay dependent on said chip rate, and a phase discriminator associated with each delay element.

3. (currently amended) The apparatus as claimed in Claim ~~2~~ 41 wherein a length of cabling is placed between said combiner and said splitter.

4. (original) The apparatus as claimed in Claim 3 wherein said length of cabling spans at least a portion of an antenna structure.

5. (original) The apparatus as claimed in Claim 4, further including a plurality of amplifiers each located such that said input signals pass through a respective one of said plurality of amplifiers prior to passing through said at least N number of modulators.

6. (original) The apparatus as claimed in Claim 5 wherein said input signals are forward link transmissions and said plurality of amplifiers are high power amplifiers.

7. (original) The apparatus as claimed in Claim 5 wherein said input signals are reverse link transmissions and said plurality of amplifiers are low power preamplifiers.

8. (original) The apparatus as claimed in Claim 4 wherein said input signals are forward link transmissions and said apparatus further includes a single high power amplifier for amplifying said aggregate signal, said high power amplifier located between said combiner and said length of cabling.

9. (original) The apparatus as claimed in any one of Claims 6, 7, or 8 wherein said phase discriminator is a modified Wilkinson combiner and both said modulators and said demodulators utilize an orthogonal methodology.

10. (original) The apparatus as claimed in Claim 9 wherein said orthogonal methodology includes Walsh codes.

11. (original)The apparatus as claimed in any one of Claims 6, 7, or 8 wherein said phase discriminator is a 90° hybrid and both said modulators and said demodulators utilize an orthogonal methodology.

12. (original) The apparatus as claimed in Claim 11 wherein said orthogonal methodology includes Walsh codes.

13. (original) The apparatus as claimed in any one of Claims 6, 7, or 8 wherein said phase discriminator is a modified Wilkinson combiner and both said modulators and said demodulators utilize a quasi-orthogonal methodology.

14. (original) The apparatus as claimed in any one of Claims 6, 7, or 8 wherein said phase discriminator is a 90° hybrid and both said modulators and said demodulators utilize a quasi-orthogonal methodology.

15. (canceled)

16. (currently amended) A method for processing N number of input signals having a common frequency and chip rate, said method comprising:

obtaining N number of input signals having a common frequency;

phase-shifting each one of said input signals by a respective phase shift sequence via a modulation scheme;

combining said phase-shifted signals to form an aggregate signal;

transmitting said aggregate signal across a length of cabling;

separating said aggregate signal through a demux element such that said aggregate signal is separated into constituent components each corresponding to each one of said input signals; and

demodulating each of said constituent components into N number of recovered signals each corresponding substantially identically to one of said N number of input signals;

wherein said demux element includes ~~a~~ N-1 splitters, a delay element associated with each splitter, ~~line~~ each delay element having one or more switches for switching in a delay dependent on said chip rate, and a phase discriminator associated with each delay element.

17. (previously presented) The method as claimed in Claim 16, further including between said obtaining step and said phase-shifting step, amplifying said input signal via a plurality of amplifiers.

18. (original) The method as claimed in Claim 17 wherein said input signals are forward link transmissions and said plurality of amplifiers are high power amplifiers.

19. (original) The method as claimed in Claim 17 wherein said input signals are reverse link transmissions and said plurality of amplifiers are low power preamplifiers.

20. (original) The method as claimed in Claim 16 wherein said input signals are forward link transmissions and said method further includes between said combining step and said transmitting step, amplifying said aggregate signal via a single high power amplifier.

21. (original) The method as claimed in any one of Claims 18, 19, or 20 wherein said phase discriminator is a modified Wilkinson combiner and said modulation scheme utilizes an orthogonal methodology.

22. (original) The method as claimed in Claim 21 wherein said orthogonal methodology includes Walsh codes.

23. (original) The method as claimed in any one of Claims 18, 19, or 20 wherein said phase discriminator is a 90º hybrid and said modulation scheme utilizes an orthogonal methodology.

24. (original) The method as claimed in Claim 23 wherein said orthogonal methodology includes Walsh codes.

25. (original) The method as claimed in any one of Claims 18, 19, or 20 wherein said phase discriminator is a modified Wilkinson combiner and said modulation scheme utilizes a quasi-orthogonal methodology.

26. (original)The method as claimed in any one of Claims 18, 19, or 20 wherein said phase discriminator is a 90º hybrid and said modulation scheme utilizes a quasi-orthogonal methodology.

27. (currently amended) An apparatus for processing N ~~number of~~ modulated input signals having a common frequency, said apparatus comprising:

a demux element for demultiplexing an amplified aggregate signal consisting of modulated forms of said input signals to output N signals,

N demodulators, each demodulator for demodulating a corresponding one of said N signals to produce N output signals, each corresponding to one modulated input signal,

said demux element including ~~a high power Walsh code discriminator, which~~ cascading stages, with each stage comprising~~es~~:

a splitter for splitting said aggregate signal into two signals ~~N number of signal components each corresponding to one modulated input signal~~;

a delay element ~~line~~ having one or more switches, said delay element adding a differential amount of delay between said two signals ~~line~~ for filtering outputs of said splitter into odd and even groups of frequencies said amount of differential delay dependent on the modulation rate used to modulate said N modulated input signals ~~of said N number of signal components~~; and

a phase discriminator for grouping said odd and even frequencies. ~~; and~~

~~N number of demodulators, each demodulator for demodulating a corresponding one of said odd and even groups of frequencies.~~

28. (original) The apparatus as claimed in Claim 27 wherein said phase discriminator is a modified Wilkinson combiner and said demodulator utilizes an orthogonal methodology.

29. (previously presented) The apparatus as claimed in Claim 28 wherein said splitter and said switches are arranged to form a comb filter.

30. (original) The apparatus as claimed in Claim 27 wherein said phase discriminator is a 90° hybrid and said demodulator utilizes an orthogonal methodology.

31. (previously presented) The apparatus as claimed in Claim 30 wherein said splitter and said switches are arranged to form a comb filter.

32. (original) The apparatus as claimed in Claim 27 wherein said phase discriminator is a modified Wilkinson combiner and said demodulator utilizes a quasi-orthogonal methodology.

33. (original) The apparatus as claimed in Claim 27 wherein said phase discriminator is a 90° hybrid and said demodulator utilizes a quasi-orthogonal methodology.

34. (new) An apparatus as claimed in claim 2 wherein said N-1 splitters, delay elements and phase discriminators are arranged in cascaded stages to sequentially split said aggregate signal into said N number of recovered signals.

35. (new) An apparatus as claimed in claim 34 wherein each delay element comprises:

a first transmission line for transmitting a first output from its associated splitter;

a second transmission line and a delay line associated with said second transmission lines for transmitting a second output from its associated splitter; and

one or more switches for switching a signal between said delay line and said second transmission line for controllably adding said delay between said first and second outputs.

36. (new) An apparatus as claimed in claim 35 wherein said delay introduced by each delay element is also dependent on the stage of said delay element.

37. (new) An apparatus as claimed in claim 36 wherein said delay introduced by the first delay element is equal to ½ of the chip rate.

38. (new) An apparatus as claimed in claim 37 wherein the delay introduced by the each subsequent delay element is equal to ½ of the delay introduced by the immediately proceeding delay element.

39. (new) An apparatus as claimed in claim 36 wherein said first transmission line introduces a fixed amount of delay equal to ½ of the delay introduced by an immediately proceeding delay element to said first output, with the first such delay element introducing a delay equal to ½ of the chip rate; and second transmission line introduces a minimal delay, and said delay line introduces the same amount of delay as said first transmission line, such that said delay is equal to the amount of delay introduced by said first transmission line when said switch is set in one position, and is equal to minimal delay when said switch is set in the other position .

40. (new) An apparatus as claimed in claim 39 wherein said switch is set in one position for one of two differential delay states in each slow chip period and the other position for the other differential delay state as required by the timing required to time shift one of the two split signals paths in each demodulator element by said differential delay with respect to the other path such that the sum of the two time periods equals the slow chip period.

41. (new) An apparatus as claimed in claim 37 wherein said apparatus is configured for a 3-sector base station with N=3 such that said demux element includes a first and second splitter, and wherein said first delay element is associated with said first splitter and wherein a second delay element associated with said second splitter introduces a delay equal to ¼ of the chip rate.